a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

C1 Cont.

a first implant junction area located in said substrate assembly beneath said first gap and extending partially beneath said gate and said source;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in said substrate assembly beneath said second gap and extending partially beneath said gate and said drain.

125. (Twice Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in said substrate assembly beneath said first gap and extending partially beneath said gate and said source, wherein said first junction area includes doped silicon areas;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap

and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

C2 Cont'd

a second implant junction area located in said substrate assembly beneath said second gap and extending partially beneath said gate and said drain, wherein said second junction area includes doped silicon areas.

128. (Twice Amended) A transistor formed on a substrate assembly, comprising:

Twice D'd C3 Cont'd

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in said substrate assembly beneath said first gap and extending partially beneath said gate and said source, wherein said first junction area includes a pocket implant junction;